MEASUREMENTS OF SPECIFIC ELECTRICAL CONTACT RESISTANCE BETWEEN SIC AND LEAD-LITHIUM EUTECTIC ALLOY

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Silicon Carbide (SiC) has been proposed as a possible candidate material for flow channel inserts for the dual coolant blanket concept. Here, the total electrical resistance of disks of high purity CVD SiC were measured with liquid lead-lithium eutectic (LLE) alloy melts serving as electrodes. From this data, the relative contributions of intrinsic resistivity and surface contact resistance as a function of measurement temperature was deduced. It was shown that after a relatively short period of exposure, once wetting at the interface was achieved, that contact resistance at the SiC/LLE interface was not significant. The contact resistance during initial exposure did not behave in a repeatable consistent way and appears to be affected by small variations in sample preparation. For modeling purposes, the electrical properties of an FCI can be based on the intrinsic electrical conductivity of the material and the dimensions. However, longer term operations and effects of impurities still need to be addressed.

I. INTRODUCTION

In the Dual Coolant Lead Lithium (DCLL) blanket [1,2] concept, silicon carbide (SiC) based flow channel inserts (FCIs) provide both electrical and thermal insulation between a flowing lead-lithium eutectic (LLE) alloy coolant and breeder region, and a helium-cooled ferritic/martensitic steel blanket structure. Overall research and development status of the DCLL concept in the USA are reviewed in Ref. [3], where issues associated with the FCI are of primary concern.

FCIs must exhibit low transverse electrical and thermal conductivity and must be compatible with LLE up to relatively high temperatures (~800°C). Electrical conductivity measurements on some candidate SiC materials have been reported [4] where the effects of neutron irradiation were also investigated. In addition, static exposure tests with LLE [5] have indicated that high purity SiC fabricated by chemical vapor deposition (CVD) is compatible with LLE below 1000°C. However, relatively poor wetting between CVD-SiC and LLE could impact the electrical contact resistance and thus the overall electrical conductance through the flowing LLE and the FCI. In addition, SiC is a semiconductor material that when coupled with a metal can exhibit rectifying diode behavior as charge carriers must traverse a Schottky barrier to flow from a metal electrode into the SiC [6]. In particular, nickel electrodes, and certain preparation and heat treatment steps, are seen to give good Ohmic contacts to SiC, with symmetric and linear *I-V* characteristics. No data were found for lead or lithium. The presence of poor wetting and contact resistance is not necessarily detrimental for FCI applications. To accurately perform calculations of magnetohydrodynamic flow phenomena that strongly influence the pressure and transport of heat and mass in the DCLL [7,8], it is important to characterize the contribution to total FCI resistance coming from contact resistance.

This paper reports on an experimental study to characterize the contribution of surface contact resistance between LLE (nominally 15-17 at% lithium for fusion) and CVD SiC. Measurements of total sample resistance are performed, and electrical conductivity and specific contact resistance are determined based on the following definition:

$$R = \frac{2r_c}{A} + \frac{t}{\sigma A}, \qquad (1)$$

where R is the sample resistance (Ω), r_c is the specific contact resistance ($\Omega.m^2$) between the sample and LLE, t is the sample thickness (m), A is the sample area (m^2), and σ is the intrinsic electrical conductivity (1/(Ω.m), or S/m) of the sample material. The factor of 2 comes from the fact that there are two interfaces through which current will cross.

II. EXPERIMENTAL PROCEEDURE

II.A. Measurement apparatus

The DC electrical resistances of disk samples of CVD-SiC were measured using a two point technique with LLE serving as the electrodes in contact with SiC. The simple apparatus is shown in Fig. 1. The disk holder and reservoir chambers pictured were made from MACOR (roughly 46% SiO_2, 17% MgO, 16% Al_2O_3, 10% K_2O, 7% B_2O_3, 4%F) chosen for its good heat resistance and ease of machining.

The DC test circuit is pictured in Fig. 2. A DC current was passed into the LLE melt, though the sample, and into the LLE melt on the opposite side. A calibrated resistor was used to measure the test current. Temperatures and voltages were measured with an Agilent 34970A Data Acquisition Unit, the adjustable DC power supply is an EPSCO Model EC-2. Test currents in the range of 20 to 80 mA were used in most cases, giving a similar current density to the in-service conditions as an FCI. ANSYS calculations indicate that, due to the relatively high conductivity of the LLE compared with that of the SiC, the current should be quite uniform in the test sample. J-type thermocouples with insulated stainless steel sheaths were used to measure the temperature in both LLE melts. The floating sheaths were used as leads by which to measure the voltage across the sample. The sample resistance, which will include contact resistance between the LLE and the SiC sample in addition to the intrinsic resistance of the SiC sample itself, was calculated as the ratio of the test voltage to test current.

The CVD-SiC samples obtained from Rohm & Haas, were classified as High Resistivity Grade SC-001. The sample disks were 25.3 mm diameter and nominally 1, 2, and 3 mm thick. Samples were ground to 0.5 μm surface roughness and were cleaned before testing with a mild acid/ethanol solution and rinsed with ethanol. The samples were cemented into the holder using RESBOND 907 fireproof adhesive. The joint was inspected under magnification before and after exposure to look for any flaws that might allow LLE penetration.

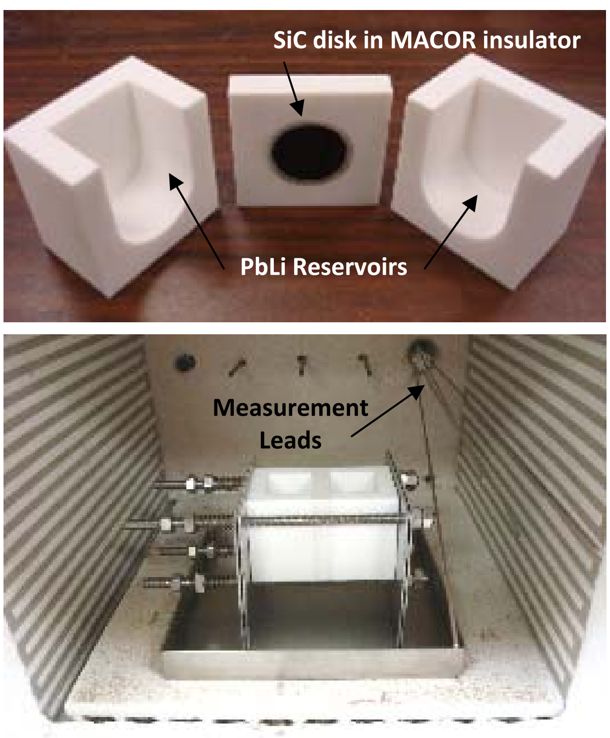

Fig. 1. LLE/SiC DC resistance measurement apparatus in pieces (above) and partially assembled furnace (below).

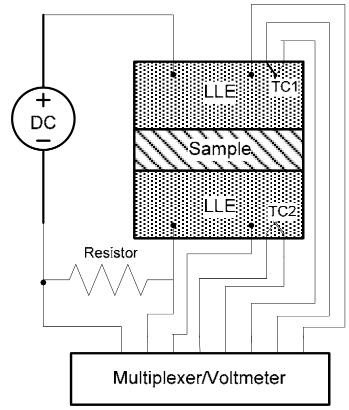

Fig. 2. DC resistance test circuit with LLE electrodes

The LLE used in these experiments was commercially available from Atlantic Metals. Measurements indicated it had 14-15 at% Li and relatively high oxygen impurity content as received from the manufacturer. The LLE melting point is nominally 235°C.

The testing was performed in an atmosphere-controlled oven under an argon purge, although significant oxygen was probably still present. The oven and sample were baked for 2 hours at 250°C in order to remove most water or hydrocarbons before LLE was introduced to the reservoirs. The oven was then opened briefly to add and stir the LLE in the reservoirs, then resealed and repurged before heating up to ~500°C.

II.B. Determination of Contact Resistance

Originally, it was planned to measure the resistances of samples with different thicknesses and then use Eq. 1 to determine the values of r_c and σ. However, measurements indicated that (1) contact resistance itself is very sensitive to surface preparation, and (2) the intrinsic conductivity of the material can vary even for material taken from the same lot. Rohm & Haas confirmed that σ for grade SC001 can vary from 0.005 to 10 S/m at room temperature, with roughly 90% of lots being < 0.1 S/m.

Instead, after conductivity testing, some disks were cut into bar samples. The conductivity was measured using a 4-point technique that eliminates the effect of contact resistance between the current leads and the sample. The simple arrangement is shown in Fig. 3.The dimensions of the test samples were measured by micrometer and are listed in Table 1.

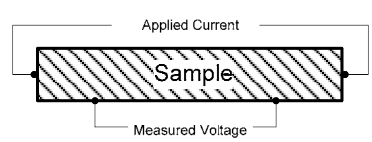

Fig. 3. DC test circuit for 4-point technique on SiC bar

TABLE I. SiC sample dimensions

Sample #	Form	Meas. Type	Thickness (mm)	x-Sectional Area (mm^2)
1	Disk	2-point LLE	3.00	506.7
1b	Bar	4-point	12.0	8.4
2	Disk	2-point LLE	1.92	506.7
3	Disk	2-point LLE	1.04	506.7
3b	Bar	4-point	14.57	1.1

III. RESULTS AND DISCUSSION

Data from Sample 1 is plotted in Fig. 4, where Eq. 1 was used to compute an effective electrical conductivity assuming no contact resistance for either the disk in contact with LLE or the bar sample measured with the 4-point technique. For comparison, data from Youngblood [9] on the same type material (but from a different lot) is also plotted. The intrinsic conductivity of the Sample 1 material as measured by the 4-point technique (1b) was relatively close to Youngblood.

In the temperature range below 400°C, the effective conductivity of Sample 1 in contact with LLE showed a lower conductivity by a factor of ~2-4 compared to the 4 point bar sample, indicating there was contact resistance making up an appreciable portion of the total resistance. However, as the sample was heated over a roughly 1-hour period, this effective conductivity of Sample 1 approached that of the 4-point measurements and those of Youngblood. Above about 450°C, the conductivity as measured in contact with LLE came within about 10-20% above/below that of that measured with the 4-point technique, indicating that the contact resistance had essentially disappeared. When Sample 1 was cooled from 500 to 400°C over a roughly 2 hour period, the conductivity stayed very close to the 4-point data indicating that LLE remained in good electrical contact with the SiC.

Using the data from the Sample 1 cooling curve, a fit to an Arrhenius type equation was constructed to approximate the actual intrinsic electrical conductivity of the material. The parameters that give minimum RMS error were determined to be:

$$\sigma_{S1} = 390.1 \cdot \mathrm{Exp}(-2457 / T[K]) , \qquad (2)$$

which gives an activation energy $E_a = 0.212$ eV.

The effective electrical conductivity for Sample 2 (again assuming no contribution from r_c in Eq. (1)) is plotted in Fig. 5 alongside the Sample 1 Arrhenius fit and 4-point data for comparison. Again the data during heating data showed significant contact resistance, more than observed for Sample 1. And again, as the sample was heated to 500°C the data approach very closely the expected value as indicated by Sample 1 data. It was assumed that this material was in fact very similar to Sample 1 material; however no confirmatory 4-point measurements were performed on Sample 2.

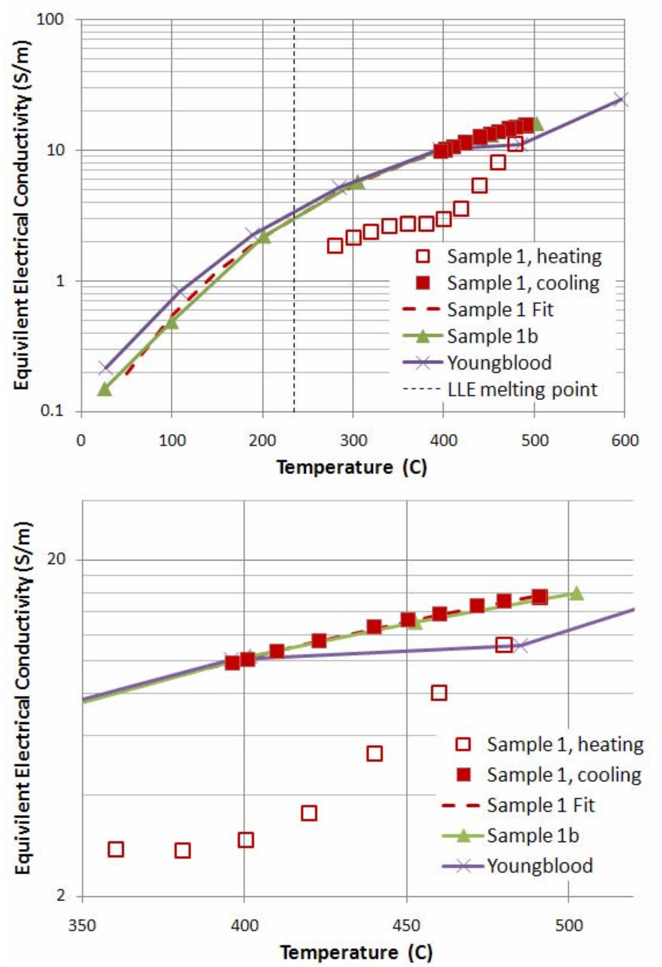

Fig. 4. Equivalent electrical conductivity of Sample 2 assuming $r_c = 0$ in Eq. (1). The data were measured during the initial heat up to ~500C (open symbols), and then upon cooling (closed symbols). For comparison, Youngblood and bar Sample 1b are also shown: Full temperature range (above), reduced range (below).

Once at 500°C, the testing current used to calculate the resistance of Sample 2 was varied from the nominal 20 mA to 60 mA. No variation of the resistance was observed over this current range, and so the contact appears to be a good Ohmic contact.

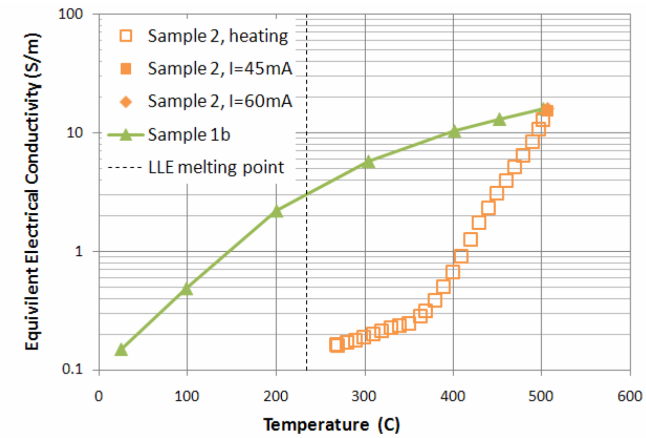

Fig. 5. Equivalent electrical conductivity of Sample 2 assuming $r_c = 0$ in Eq. (1).

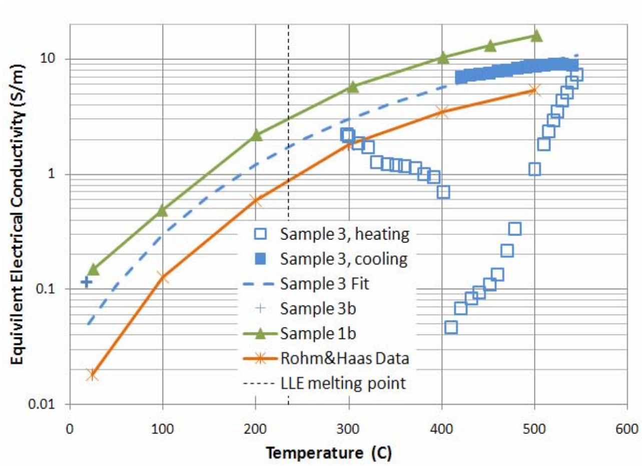

Fig. 6. Equivalent electrical conductivity of Sample 3 assuming $r_c = 0$ in Eq. (1).

The effective electrical conductivity for the nominally 1 mm thick Sample 3 is plotted in Fig. 6 alongside the Sample 1 4-point data and data from Rohm & Haas [10] typical of high resistivity grade CVD SiC material for comparison. Again the data during heating data showed significant contact resistance, but with an odd non-monotonic response to increasing temperature (and time). It should be noted that in the preparation of this test, the reservoirs containing the LLE in contact with either side of the sample were vigorously stirred when first filled to try to promote good early contact of the melt with the SiC. This appeared to give initial contact closer to Sample 1 rather than Sample 2. However, the contact resistance then increased as the sample was heated. This trend reversed around 400°C and contact resistance decreased with further heating. Sample 3 was heated about 40°C hotter than the previous tests to help promote good contact. However, the final value of the effective conductivity was half of that measured for Samples 1 and 2.

The data taken during cooling had a similar behavior as Sample 1. The best fit to the Sample 3 cooling data, assuming the same activation energy as Sample 1 (see Eq. (2)) was also plotted in Fig. 6. The same activation energy is chosen after comparing against the Rohm & Haas data, which also demonstrates similar activation energy. It is noted that the slope of the fit equation and the data do not match exactly. Sample 3 was then cut into a bar sample and tested by the 4-point method. The data at room temperature for this Sample 3b agree with Sample 1, and not with the Sample 3 fit (technical difficulties with contacts were encountered when trying to measure Sample 3b via the 4-point method at elevated temperatures – those data are not yet available). It is tentatively concluded that the Sample 3 disk intrinsic electrical conductivity are the same as Samples 1 and 2, and that even during testing in contact with LLE up to 540°C, contact resistance was not fully eliminated.

Using Eqs. 1 and 2, and the raw resistance data for the disks, an estimate of the specific contact resistances, r_c, are calculated and plotted in Fig. 7. In all cases, as the temperature (and time) of the exposure is increased, the contact resistance is reduced. In Samples 1 and 2 r_c is reduced to a relatively low value, and the contribution of the intrinsic resistance of the material itself dominates the total resistance. However, Sample 3 still shows appreciable contact resistance even at the peak temperature. Additionally each sample behaves differently following initial contact with the LLE at temperatures near the LLE melting point, indicating that electrical contact is sensitive small changes in initial surface and/or LLE melt conditions. This variation made it impossible to simply compare samples of different thickness over the whole temperature range in order to determine the relative contribution of r_c. A similar sensitivity when using solid metal electrodes is noted by Youngblood in his tests [11], and is certainly documented in the semiconductor industry where very low r_c is the goal [6].

Following the roughly day long exposure of each sample during which the measurements were conducted, the SiC surface exhibits some greenish scale formation, pictured in Fig. 8. This scale appears to be heavier than reported in Pint [5] where a thin oxide film is present and surface analysis by X-ray Diffraction Spectroscopy indicated some small Li presence. The exposure conditions in Pint [5] were very well controlled, where in these experiments there is expected a residual amount of oxygen available in the oven, as well as possible fluorine from the MACOR sample holder. Samples that were retested without removal of the scale showed consistently higher resistance, by an order of magnitude or more than the virgin samples. Even samples scoured with sandpaper and washed with acid/ethanol solution showed a higher resistance by roughly a factor of two compared to the virgin surfaces, even at 500°C.

IV. CONCLUSIONS

Measurements of the resistance of CVD SiC disk samples of different thicknesses in contact with lead-lithium (Pb-15Li) eutectic alloy were made and compared to each other, and to 4-point conductivity measurements of bar samples of the same material, in order to determine the relative contribution of contact resistance at the SiC/LLE interface. Significant contact resistances ranging from 10^{-4} to 10^{-2} Ω.m^2 were seen when samples first came in contact with LLE near its melting point, but generally decreased as the sample was heated over the period of ~1.5 hours. The behavior of the contact resistance during the heating cycle varied from sample to sample and was not quantitatively repeatable, presumably depending on small variations in disk preparation and LLE introduction and stirring. Variation in electric current did not reveal any non-Ohmic effect at the interface.

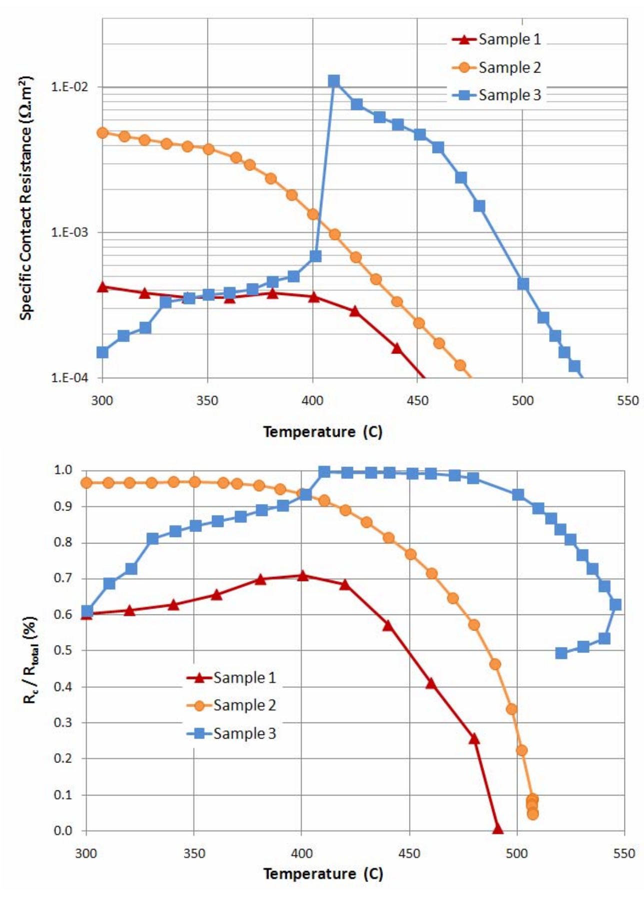

Fig. 7. Specific contact resistance of test samples using estimates of intrinsic electrical conductivity measured on Sample 1b: absolute r_c (above) and percentage of total sample resistance due to contact resistance (below).

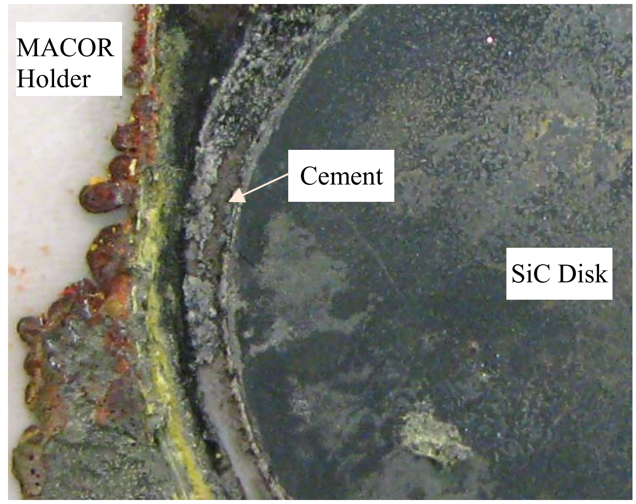

Fig. 8. Image of portion of SiC disk and MACOR sample holder showing greenish scale on SiC and colorful compounds formed by LLE attack on the MACOR.

After day long exposures, a scale of material was observed on the SiC samples, and repeated tests using the same sample exhibited higher contact resistance that did not disappear within the test temperature range with maximum 500°C. The presences of impurities in the furnace atmosphere and in the LLE itself may be main reason for this scale formation, but this remains to be established conclusively.

In regards to the application of SiC as a flow channel insert material for the DCLL blanket, it appears that increased FCI resistance due to contact resistance at the SiC/LLE interface is generally not significant after a relatively short period of high temperature exposure. Even the one sample that showed some residual contact resistance at 540°C still had an absolute value after exposure of $r_c < 3 \times 10^{-5}$ Ω.m^2. For an FCI with a thickness of 5 mm, this degree of surface contact resistance amounts to roughly a 13% increase. Estimating the FCI electrical properties using only the intrinsic conductivity of the SiC materials appears justified at this time. Future work should attempt to establish the conditions of the SiC/LLE interface over longer periods of time with prototypic materials and control of impurities in the system in such a way to be consistent with its fusion application.

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